REMARKS

In the specification, the paragraph at page 23, line 15, has been amended to correct minor editorial problems.

Claims 8-26, 29-32, 34-36 and 39-47 remain in this application. Claims 1-7, 27, 28, 33, 37, and 38 have been cancelled without prejudice.

In the previous Response to Office Action, Applicants pointed out that pending claim 12 has not been rejected or objected to the Examiner. In the current Office Action, the Examiner has not rejected or objected to pending claim 12. Claim 12 has been rewritten to include the limitations of base claim 8. Applicants believe claim 12 to be allowable.

The Examiner has indicated that claim 18 to be allowable if rewritten to include the limitations of the base claim. Paragraph 5 of the Office Action indicates claim 8 to be allowable; however, the Applicants believe this is a typographical error by the Examiner, since claim 18 in the Office Action Summary is particularly objected to, and claim 8 is rejected under 35 U.S.C. §103. Claim 18 has been rewritten to include the limitations of base claim 15. Applicants believe claim 18 to be allowable.

Claims 12 and 18 are thus allowable, and are not discussed in the following remarks.

35 U.S.C. §103

Claims 8-11, 13-14, and 39-47 are rejected under 35 U.S.C § 103 as being unpatentable over U.S. Patent 5,680,354 by Kawagoe (Kawagoe), in view of U.S. Patent 5,730,830 to Yasuhiro (Yasuhiro).

Independent claim 8 recites:

> a first XOR circuit having a first input to receive first data in a first format, a second input to receive a periodic signal other than the first data; and an output to provide the first data in a second format; and
>
> a second XOR circuit having a first input coupled to the output of the first XOR circuit, a second input coupled to receive the periodic signal other than the first data, and an output to provide the first data in the first format.

Kawagoe does not suggest or teach that either of the first or second XOR circuits receives a "periodic signal" as an input. The Office Action concludes that signal S2 of Kawagoe's Fig. 1 is a "periodic address signal."

In the field of electronics, however; the term "periodic signal" is understood to mean a signal that repeats at a regular interval or "period." The square wave 47 shown in Fig. 3 of this application is one example of such a periodic signal. Kawagoe's signal S2, on the other hand, does not repeat at a regular interval—and indeed the Examiner has not argued such. Rather, as the Examiner states, it "outputs an output signal S2 at an 'H' level if buffer output signals A0, . . . , An, /A0, . . . , /An match a registered address."

Thus, Kawagoe's "circuit 4" receives addresses, compares them to addresses of defective cells, and outputs a true signal at S2 if a particular address corresponds to a defective cell. Because the occurrence of defective cells is random, signal S2 has a random timing depending on the locations or addresses of defective cells. Being random, S2 cannot be considered a "periodic signal" in accordance with the accepted usage of that term.

Furthermore, it is apparent that the invention of Kawagoe would be inoperative if S2 were to change at a regular period.

Thus, the XOR circuits of Kawagoe's Fig. 1 do not receive a "periodic signal" as argued by the Examiner. Since claim 8 recites that inputs of the first and second XOR circuits receive a periodic signal, and since Kawagoe does not

show or suggest such an arrangement, claim 8 the rejection of claim 8 is unsupported by the prior art.

Yasuhiro is cited only in relation to the burst counter recited in claim 11, and not to show an XOR circuit that receives a periodic signal. Accordingly, neither Kawagoe nor Koshikawa suggests the particular configuration recited in claim 8.

Applicants respectfully request that the §103 rejection of claim 8 be withdrawn.

Dependent claims 9-14 are allowable by virtue of their dependency on base claim 8 and because of the additional elements recited therein. For example, claim 10 further recites that "the periodic signal comprises an address signal for addressing the memory." Signal S2 described in Kawagoe is not an address bit or an address signal. Yasuhiro is cited for teaching a burst counter, however, does not suggest or teach a periodic signal that comprises an address signal. Since neither of the cited references shows an address signal received by an XOR circuit, the rejections of these claims are improper and should be withdrawn.

Claim 11, which depends from claim 10, further recites "wherein the address signal is generated by a burst counter." As discussed, the signal S2 described in Kawagoe is not an address signal. Yasuhiro is cited for teaching a burst counter, however, a combination of Kawagoe and Yasuhiro does not suggest or teach that a burst counter may generate an address signal to be used as an input since Kawagoe does not teach that the input is an address signal.

Applicants respectfully request that the §103 rejection of claims 9-14 be withdrawn.

Independent claim 39 recites "writing data to the memory device via a first XOR circuit clocked by a periodic signal other than a data signal." As discussed, Kawagoe does not suggest nor teach the use of a period signal to clock an XOR circuit. Yasuhiro is cited for teaching a burst counter, however, does not suggest or teach the use of periodic signal as an input to an XOR circuit. Thus, applicants respectfully request that the §103 rejection of claim 39 be withdrawn.

Independent claim 40 recites "writing data to the memory device via first XOR circuit clocked by a periodic signal other than the data; and reading the data from the memory device via a second XOR circuit clocked by the periodic signal." As discussed Kawagoe does not suggest or teach the use of a periodic signal to clock an XOR circuit.

Applicants respectfully request that the §103 rejection of claim 40 be withdrawn.

Independent claim 41 recites:

> providing first data to a bus interface of the memory device in a first format and at a first data rate;
>
> reformatting the first data to a second format in response to an address signal, the second format having a second data rate different than the first data rate; and
>
> storing the first data in the memory device in the second format.

Although the Examiner has rejected claim 41 based on a combination of Kawagoe and Yasuhiro, the Examiner has not addressed the elements of claim 41 in regards to Kawagoe and Yasuhiro. In particular, the Examiner has not shown how a combination of Kawagoe and Yasuhiro would suggest or teach providing a first data at a first data rate and reformatting the first data to a second format in response to an address signal to, where the second format has a second data rate

different than the first data. Fig. 1 of Kawagoe shows a memory device 1 that receives data. Kawagoe, however, does not suggest or teach reformatting this data to a second format having a different data rate in responses to an address signal. Yasuhiro is cited for teaching a burst counter, however, does not suggest or teach reformatting data to a second format having a different data rate.

Accordingly, applicants respectfully request that the §103 rejection of claim 41 be withdrawn.

Dependent claims 42 and 43 are allowable by virtue of their dependency on base claim 41, and by virtue of the additional elements recited therein. Applicants respectfully request that the §103 rejection of claims 42 and 43 be withdrawn.

Independent claim 44 recites:

> a reformatting circuit receiving data in a first format at a first data rate from the data bus, and reformatting the data to a second format in response to an address signal on the address bus that alternates the first data rate, the reformatted data having a second data rate that is different than the first data rate; and
>
> a memory circuit coupled to the reformatting circuit and storing the reformatted data.

The Examiner has rejected claim 44 based on a combination of Kawagoe and Yasuhiro; however, the Examiner has not addressed the elements of claim 41 in regards to Kawagoe and Yasuhiro. As discussed above in relation to the allowabilitly of claim 41, the Examiner has not dealt with the particular elements regarding reformatting a data having a first data rate to a reformatted data having a second data rate. Kawagoe nor Yasuhiro suggest or teach the use of different data rates.

Applicants respectfully request that the §103 rejection of claim 44 be withdrawn.

Dependent claims 45-47 are allowable by virtue of their dependency on base claim 44 and by virtue of the additional elements recited therein. Applicants respectfully request that the §103 rejection of claims 45-47 be withdrawn.

Claims 15-36 are rejected under 35 U.S.C § 103 as being unpatentable over U.S. Patent 5,295,188 by Wilson et al (Wilson), in view of U.S. Patent 4,071,889 to Sumida et al (Sumida).

Independent claim 15 recites:

> a first circuit having a plurality of terminals; a first plurality of XOR circuits each having a first input coupled to one of the plurality of terminals, a second input coupled to receive a first periodic signal, and an output; and
>
> a second circuit having a first plurality of terminals each coupled to an output of one of the first plurality of XOR circuits, and a second plurality of terminals, wherein a number of the first plurality of terminals is different than a number of second plurality of terminals.

Wilson does not suggest or teach that first XOR circuits receive a periodic signal as an input. The Examiner asserts that "AND logic gate 64 providing [provides] an output signal, which is periodically toggling between the 'one' logic level and the 'zero' logic level (see lines 1-9, column 14)".

Although toggling does occur between the 'one" logic level and the 'zero" logic level, Wilson does not suggest that such an output signal be periodic. As discussed above in support of Claim 8, a "periodic signal" is understood to repeat at a regular interval. The output of Wilson's gate 64 does not behave in this manner. In fact, the invention of Wilson would be inoperative if the output signal were a periodic signal.

Sumida is cited only in relation to the shift register of claim 17 and not to show XOR circuits that receive a periodic signal. Accordingly, neither Wilson nor Sumida suggests the particular configuration recited in claim 15.

Applicants respectfully request that the §103 rejection of claim 15 be withdrawn.

Dependent claims 16-20 are allowable by virtue of their dependency on base claim 15 and by virtue of the additional elements recited therein.

Applicants respectfully request that the §103 rejection of claims 16-20 be withdrawn.

Independent claim 25 recites:

> a first circuit;
> a first plurality of XOR circuits having first inputs coupled to receive first data from the first circuit, second inputs each coupled to receive a bit of a first predetermined number, and outputs; and
> a second device comprising: a second plurality of XOR circuits having first inputs coupled to the outputs of the first plurality of XOR circuits, and second inputs coupled to receive one bit of the first predetermined number.

Claim 25 has been rejected over Wilson and Sumida, under the assertion that Fig. 3 of Wilson discloses "a system comprising: a first circuit 56 having a plurality of output terminals each being connected to each first input of each of a first plurality of XOR gates 74; memory 60, having a number of memory locations as matrix T which are pseudorandom numbers ..., and including AND logic gate 64 providing an output signal, which is periodically toggling between the "one" logic level and the "zero" logic level, to the second inputs of the first plurality of XOR gates 74; a second circuit comprising buffer memory circuit 78 having a plurality of input terminals connected to the outputs of the first XOR gates 74; a

second plurality of XOR gates 68 each having a first input being coupled to the second circuit buffer memory circuit 78 and a second input being coupled to the output signal from AND logic gate 64, which is periodically toggling between the "one" logic level and the "zero" logic level."

The signals received by XOR circuits 74 are dependent on words representing noise, meaning that the words and their bits can change. (See Wilson at col. 13 line 61 to col. 14 line 28). The Examiner points out that the T-Matrix generator 63 of Wilson comprise pseudorandom numbers, and as shown in Fig. 3 of Wilson such pseudorandom numbers determine input to XOR circuits 74.

Claim 25 particular recites a predetermined number which Wilson fails to suggest or teach; and in fact teaches receiving input based on a random number that represents noise.

Sumida is cited only in relation to the shift register that is not recited in claim 25 or independent claims 26-32, and not to show XOR circuits that receive a a bit of a predetermined number. Accordingly, neither Wilson nor Sumida suggests the particular configuration recited in claim 25.

Applicants respectfully request that the §103 rejection of claim 25 be withdrawn.

Dependent claims 26-32 are allowable by virtue of their dependency on base claim 25 and by virtue of the additional elements recited therein. Applicants respectfully request that the §103 rejection of claim 25 be withdrawn.

Previously amended independent claim 34 recites:

> a first circuit;
>
> a first plurality of XOR circuits having first inputs coupled to receive first data from the first circuit, second inputs each coupled to receive a bit of a predetermined number;
>
> a second circuit providing the first predetermined number to the first plurality of XOR circuits; and
>
> a second plurality of XOR circuits having first inputs coupled to outputs of the first plurality of XOR circuits, second inputs coupled to the predetermined number, and outputs coupled to the first circuit.

As discussed above, Wilson discloses inputs to XOR circuits 74 are derived from a T-matrix generator 63 that provides inputs based on noise or pseudorandom numbers. Wilson does not suggest or teach providing a "first predetermined number to the first plurality of XOR circuits" as recited by claim 25.

Sumida is cited only in relation to the shift register and not to show XOR circuits that receive a bit of a predetermined number. Accordingly, neither Wilson nor Sumida suggests the particular configuration recited in claim 34.

Applicants respectfully request that the §103 rejection of claim 33 be withdrawn.

Dependent claims 35-36 are allowable by virtue of their dependency on base claim 33 and by virtue of the additional elements recited therein. Therefore, it is respectfully requested that these claims be allowed.

Conclusion

All pending claims 8-26, 29-32, 34-36, and 39-47 are in condition for allowance. Applicants respectfully request reconsideration and prompt issuance of the subject application. If any issues remain that prevent issuance of this application, the Examiner is urged to contact the undersigned attorney before issuing a subsequent Action.

Respectfully Submitted,

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By: _____

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